REMARKS

Claims 1-20 were pending in this application.

Claims 1-20 have been rejected.

Claims 1, 2, 5, 7, 10-12, 15, 17 and 20 have been amended in this Response.

Claims 1-20 remain pending in this application.

The Applicants respectfully request reconsideration of Claims 1-20.

I. IN THE CLAIMS

Independent Claims 1 and 11 have been amended to recite limitations commensurate with the scope of the Applicants' invention. The amendments to Claims 1 and 11 and 19 do not narrow the scope of the claims. Dependent Claims 2, 5, 7, 10, 12, 15, 17 and 20 have been amended to more clearly claim the Applicants' invention.

II. REJECTIONS UNDER 35 U.S.C. § 112

The Office Action rejects Claims 2, 5, 7, 10, 12, 15, 17 and 20 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. In particular, the Office Action asserts that as per Claim 2, the recitations in lines 4-20 appear misdescriptive since they contradict the recitations in the specification and Figure 3. In response to the Examiner's rejection, the Applicants have amended Claims 2, 5, 7, 10, 12, 15, 17 and 20 to correspond to the description in the specification and the

Figures. The Applicants respectfully request the withdrawal of the rejection under 35 U.S.C. § 112.

III. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18 and 19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,638,058 to Masumoto ("*Masumoto*"). This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. §102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP §2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP §2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Masumoto describes circuitry for performing a rounding operation on a binary number. Specifically, it describes a parallel technique that determines whether to change a bit value by ANDing together all the bits of lesser significance and the rounding carry bit at the least-significant bit position. *See Masumoto, col. 3, lines 18-26.*

Regarding independent Claims 1, 6, 11 and 16, the claims recite a round off mechanism comprising an incrementer selectively incrementing an operand at a most significant discard bit position to generate an incremented intermediate rounding result. The claims further recite control logic causing the mechanism to produce a truncated remainder of either the operand or the

incremented intermediate result. Section 3 of the Office Action asserts that *Masumoto* describes an incrementer generating an incremented intermediate rounding result at column 3, lines 7-13. The Applicants respectfully submit that the cited passage actually describes a complete prior art rounding circuit and that the *Masumoto* reference in fact describes an alternative approach to such a circuit.

The cited passage (and the succeeding sentence) state:

> Rounding in binary arithmetic is performed by adding a binary "1" at a bit position one less in significance than the least-significant bit position of the desired rounded number. For example, if the least-significant bit position of the desired rounded number is fourteen, rounding can be performed by adding a "1" in the thirteenth bit position, where the bit positions are conventionally numbered from the least-significant to the most-significant. This approach to rounding causes a carry bit to ripple along the number being rounded until the first "0" bit is encountered. (*emphasis added*)

The Applicants submit that this language is virtually identical to the following passages from the description of the Background of the Invention: "Rounding may be performed by adding a "1" bit at a bit position one less in significance than the least significant bit position of the desired result." *Masumoto, col. 1, lines 14-16.* "Rounding by this process requires the rounding carry, if any, to "ripple" across the number being rounded until the first zero is encountered." *Masumoto, col. 1, lines 33-35.* Thus, the passage relied upon by the Office Action is describing a prior art circuit that performs the entire rounding process by adding a "1" bit to the number to be rounded at a specified bit position.

In order to improve upon this technique, *Masumoto* argues that "[f]or high-speed operation, some form of look-ahead rounding process is more desirable, so that the separate bits of the rounded number can be computed in parallel rather than one after the other." *Masumoto, col. 1, lines 38-42.*

The *Masumoto* circuitry provides such a look-ahead rounding circuit. *See Masumoto, col. 2, lines 6-7.*

Thus, the *Masumoto* reference does not describe a round off mechanism comprising an incrementer selectively incrementing an operand to generate an incremented intermediate rounding result and control logic causing the mechanism to produce a truncated remainder of either the operand or the incremented intermediate result, as recited in independent Claims 1, 6, 11 and 16. For these reasons, the *Masumoto* reference fails to show identically each and every limitation of the claimed invention arranged as they are in independent Claims 1, 6, 11 and 16 and, therefore, does not anticipate independent Claims 1, 6, 11 and 16 (and claims depending therefrom). Accordingly, the Applicants respectfully request withdrawal of the § 102 rejection and full allowance of Claims 1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18 and 19.

IV. CONCLUSION

For the reasons given above, the Applicant respectfully requests reconsideration and full allowance of all pending claims and that this application be passed to issue.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com.*

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: Aug. 12, 2004

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